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FIG. 3

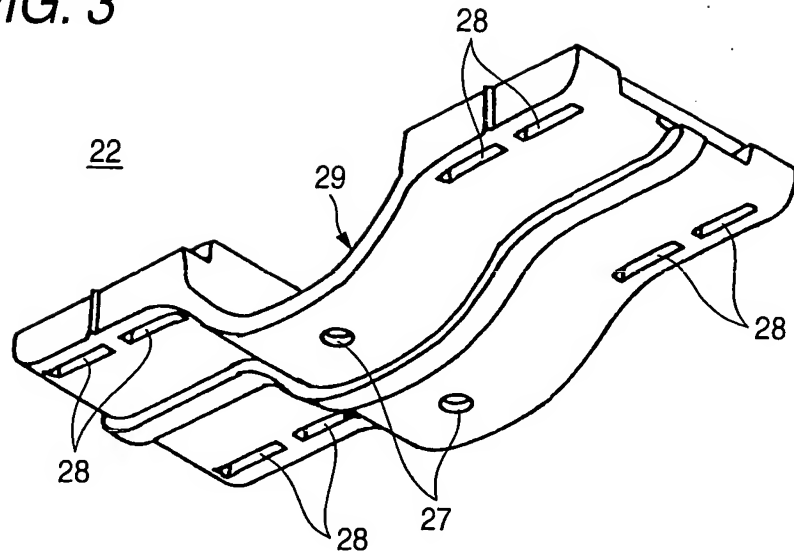
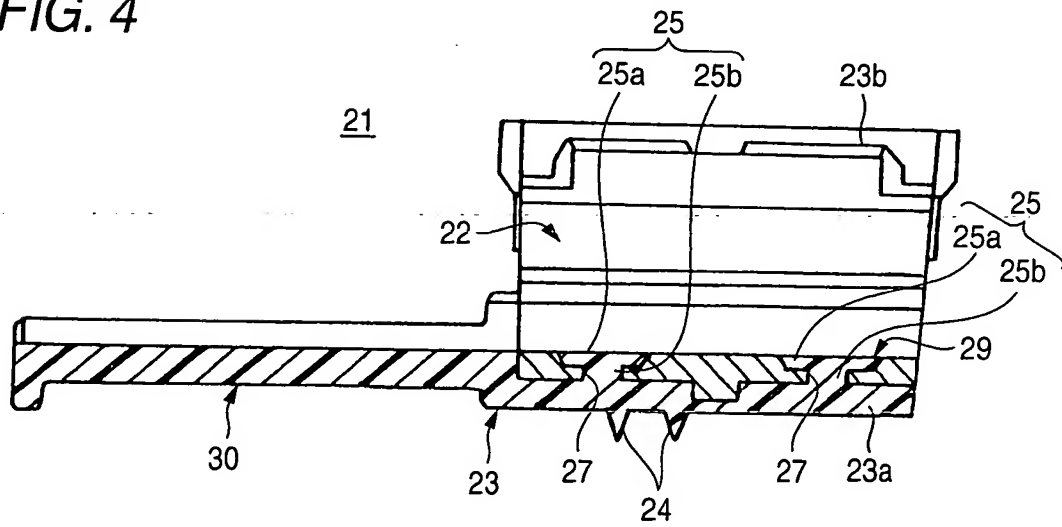


FIG. 4



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FIG. 5

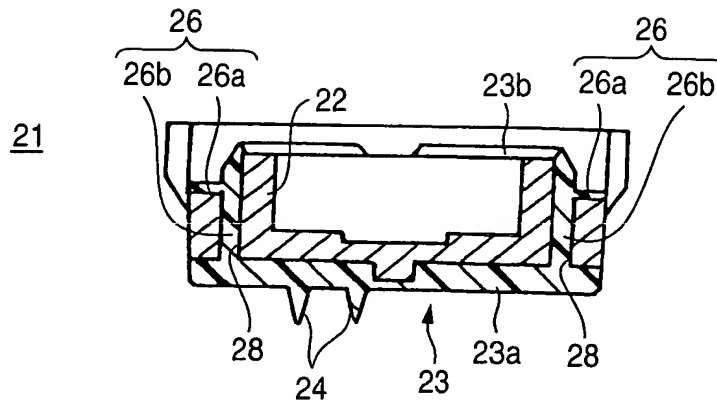
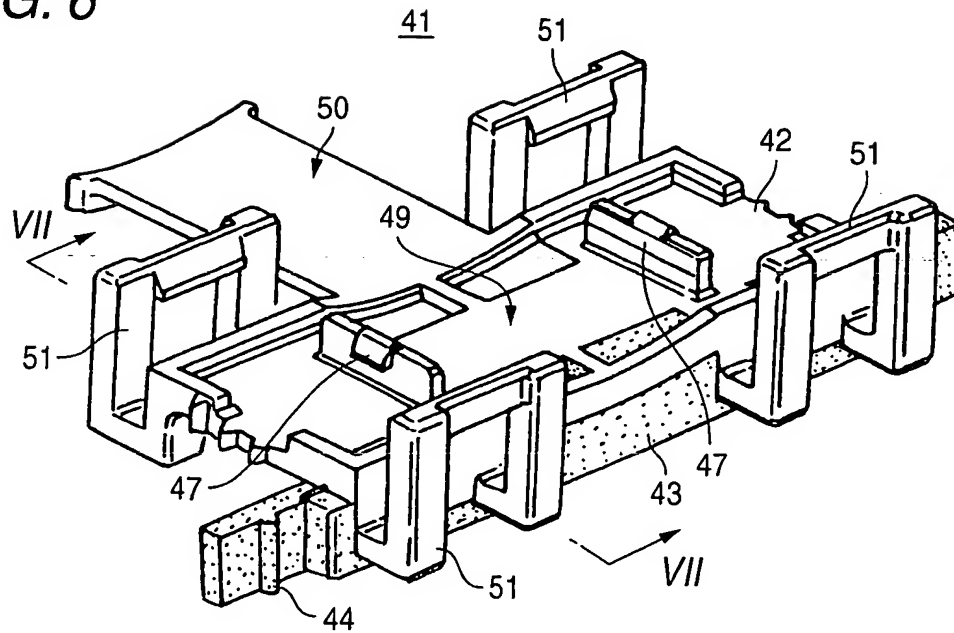
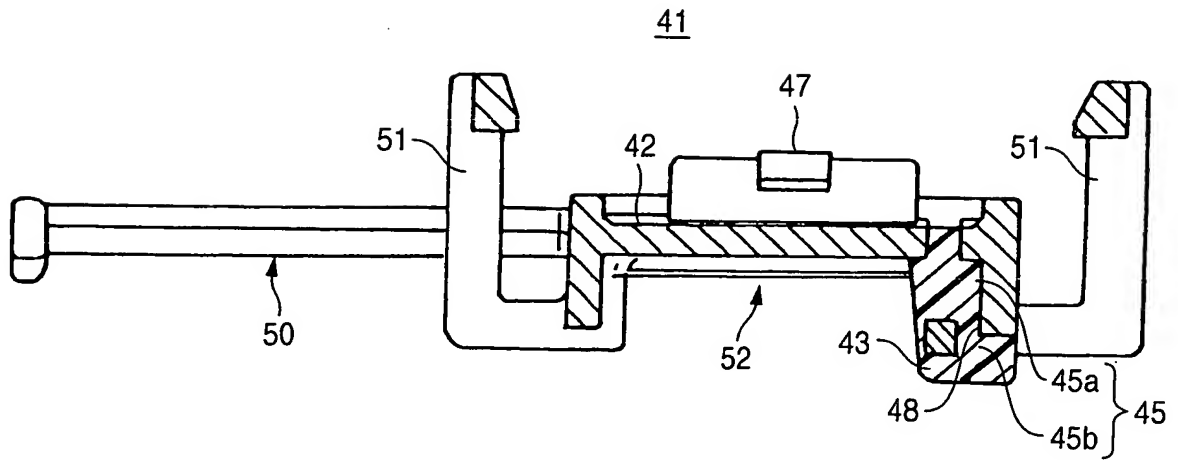


FIG. 6



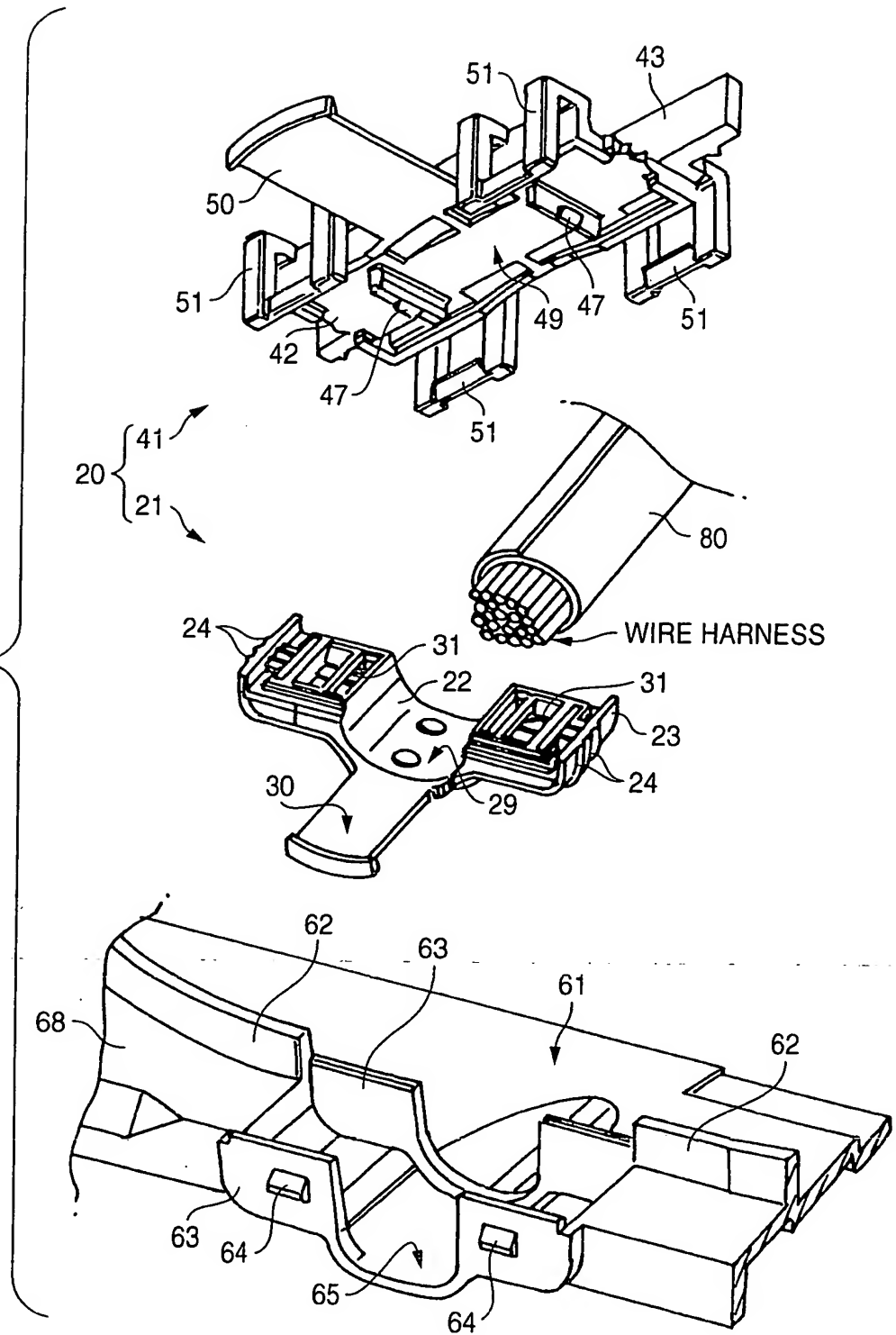
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FIG. 7



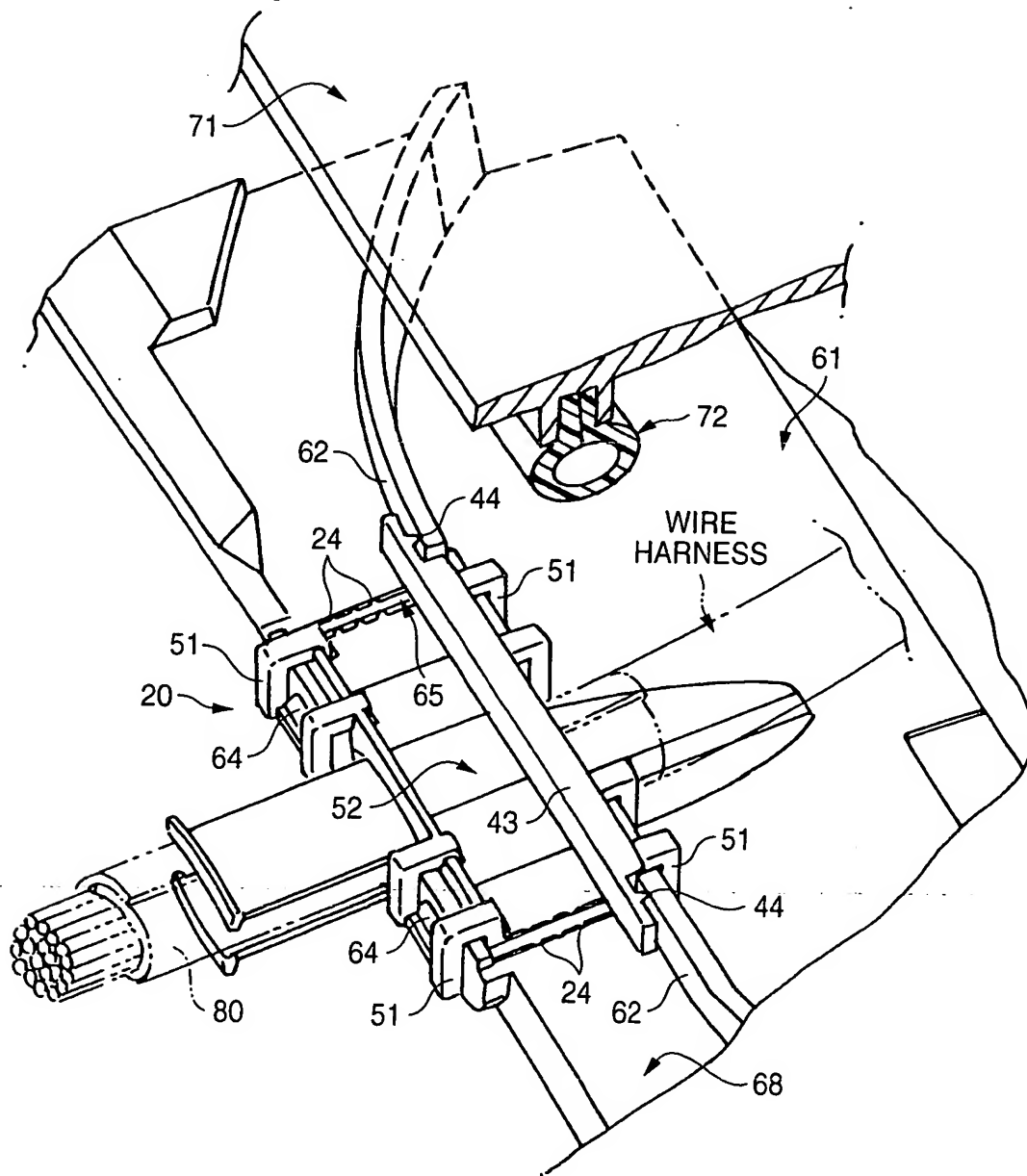
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FIG. 8



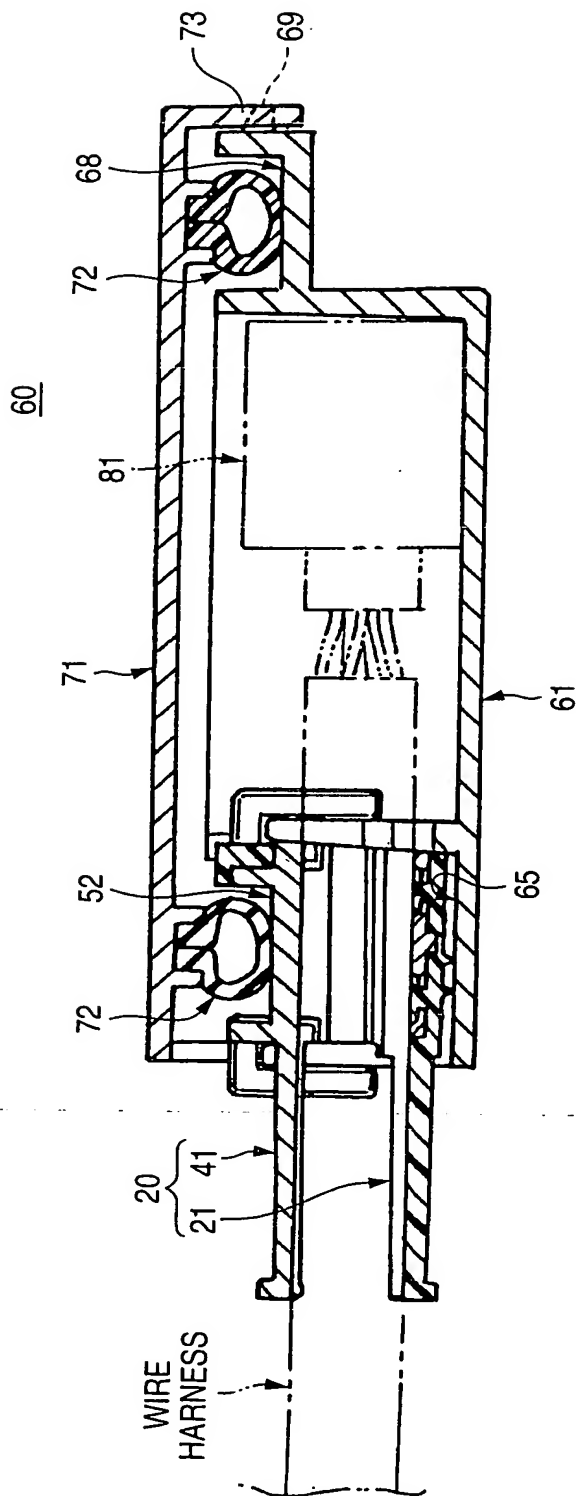
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FIG. 9



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FIG. 10

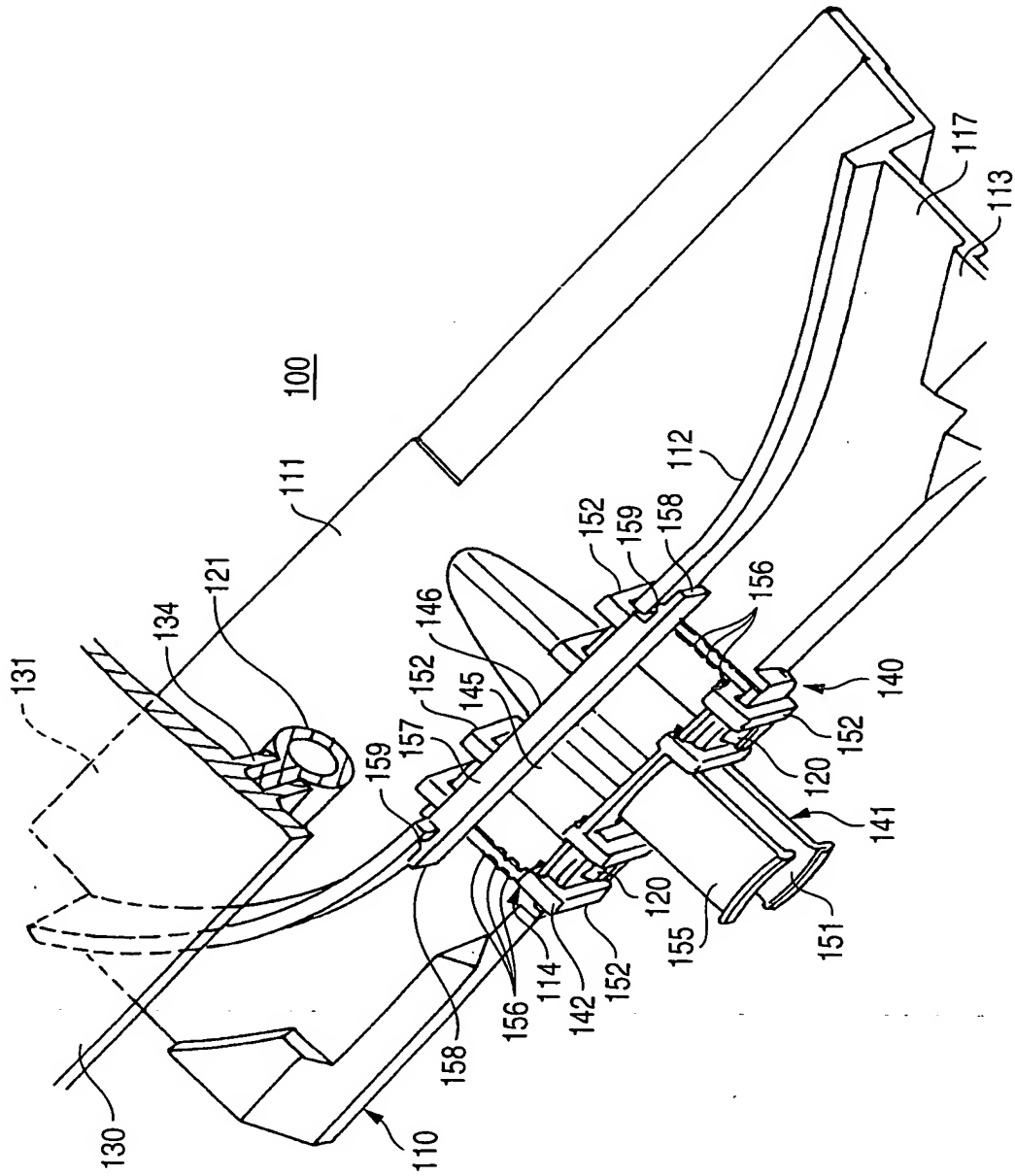


This cross-sectional view shows a semiconductor device assembly. A substrate 21 is shown with a layer 30 on its top surface. A central component 23 is mounted on the substrate, featuring a top layer 25 and a bottom layer 24. The top layer 25 is divided into two regions, 25a and 25b, which are separated by a gap. The bottom layer 24 is also divided into two regions, 25a and 25b, which are separated by a gap. The regions 25a and 25b are connected to the substrate 21 by a series of conductive layers 27. A layer 26 is located between the top layer 25 and the bottom layer 24. The substrate 21 is shown with a top surface 30 and a bottom surface 31.



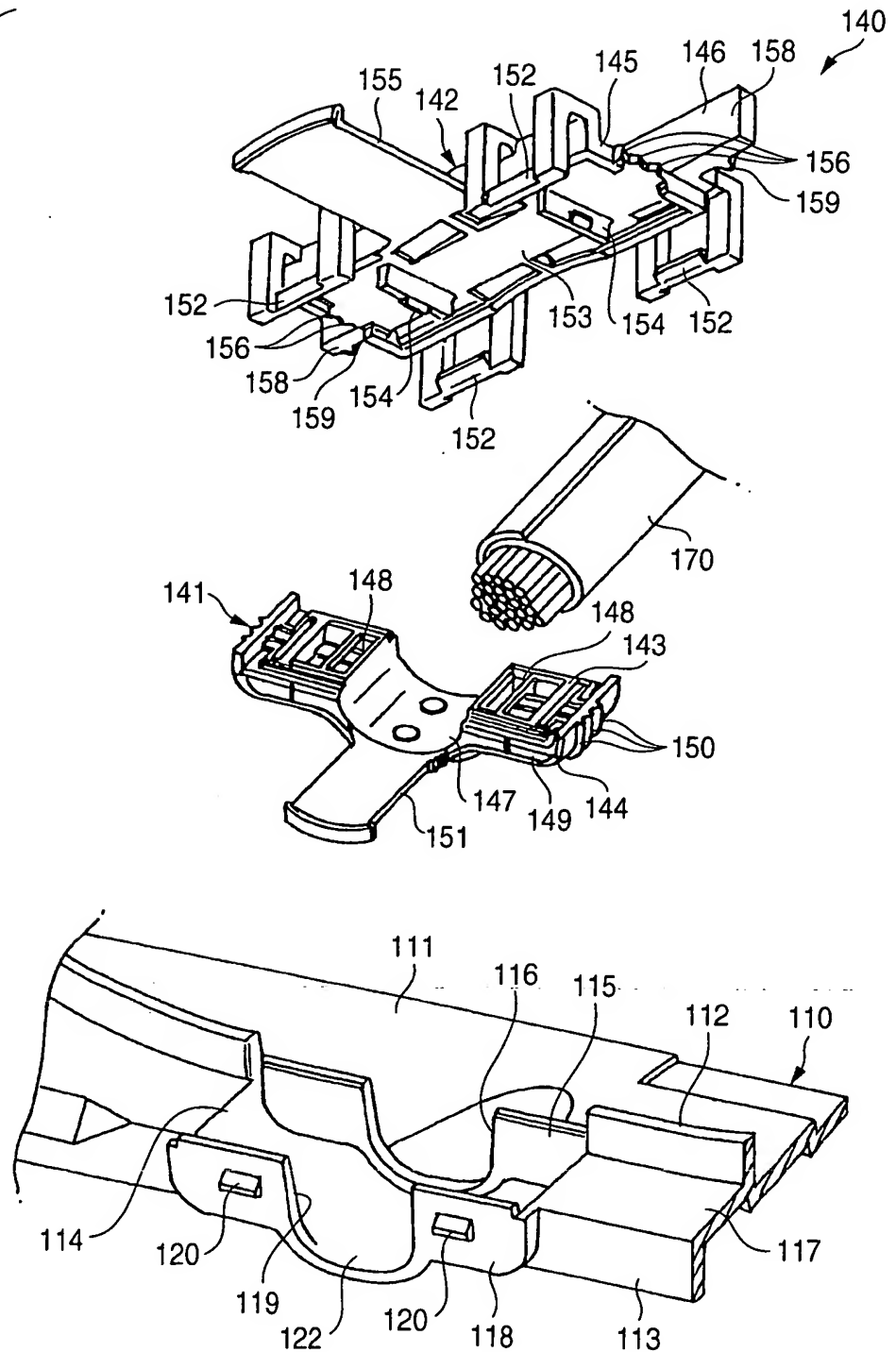
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FIG. 12



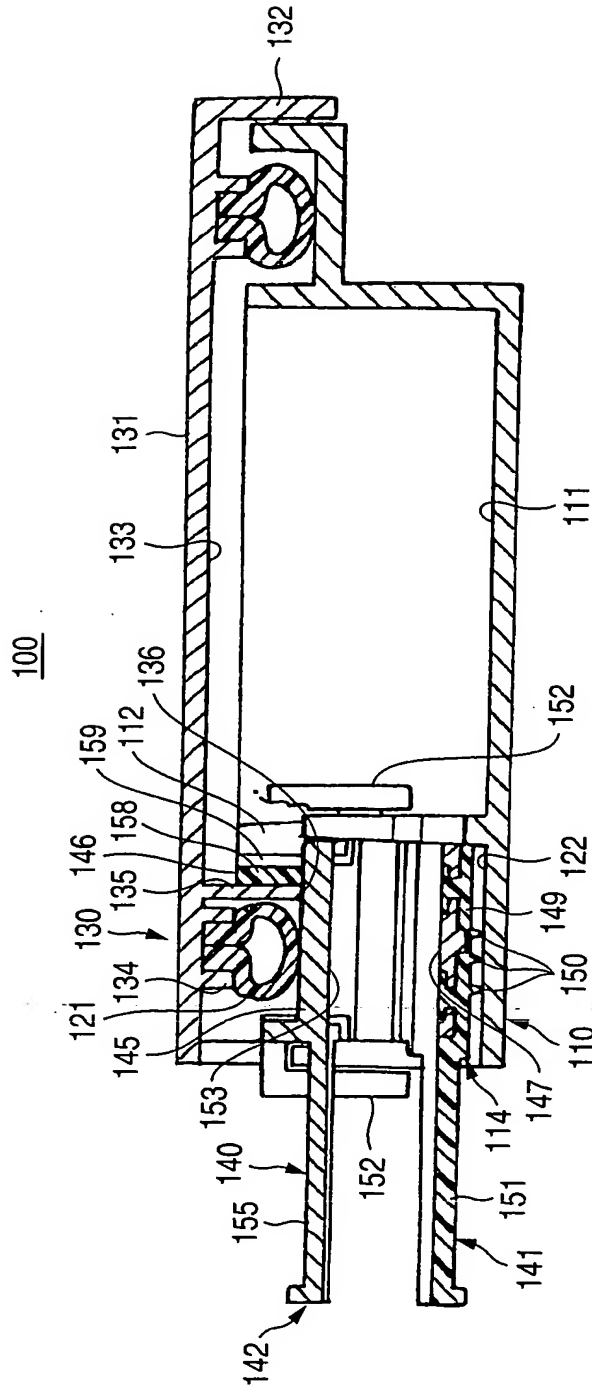
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FIG. 13



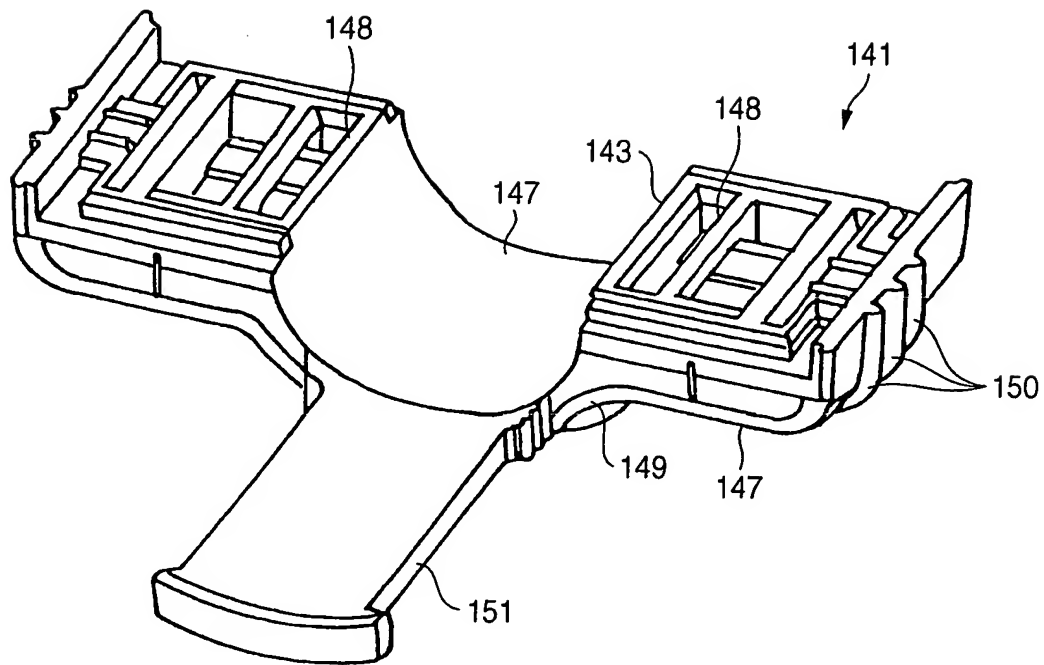
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FIG. 14



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*FIG. 15*



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FIG. 16

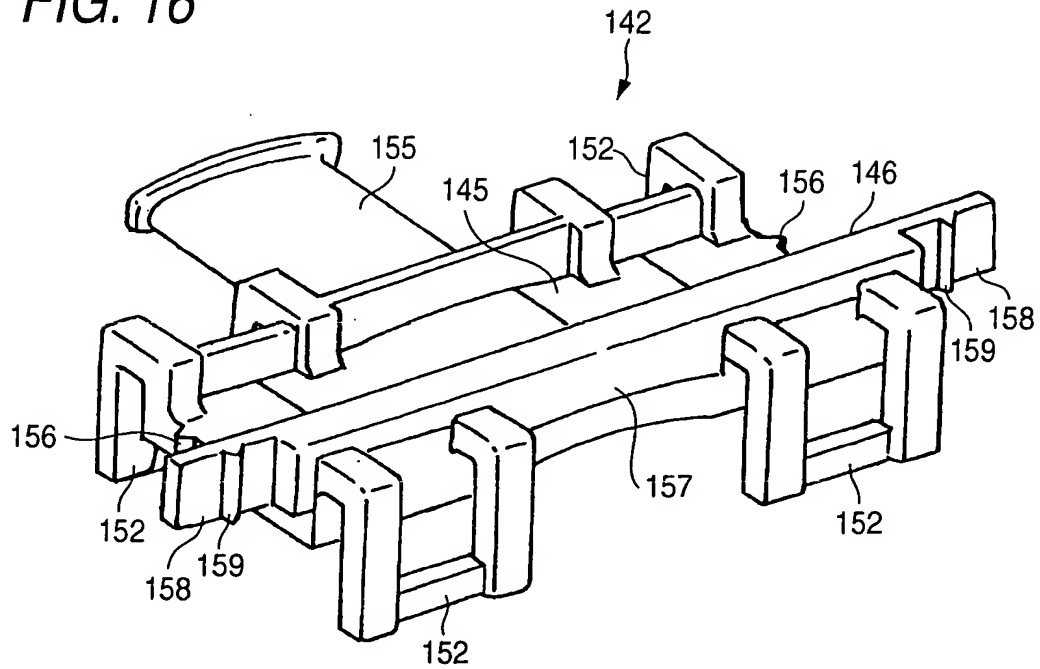
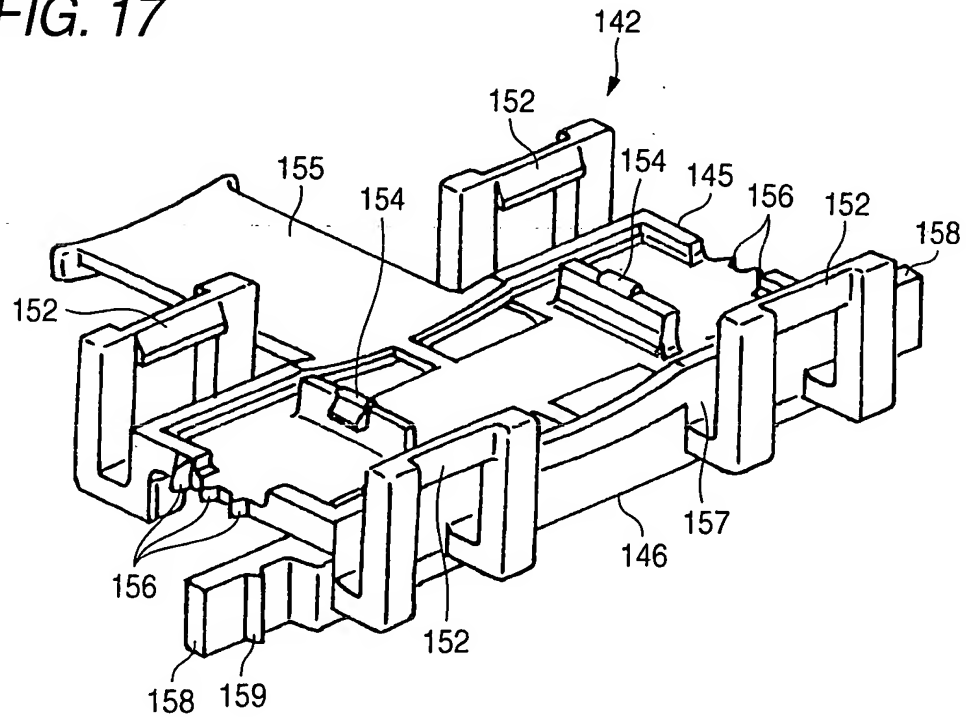
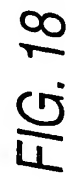


FIG. 17

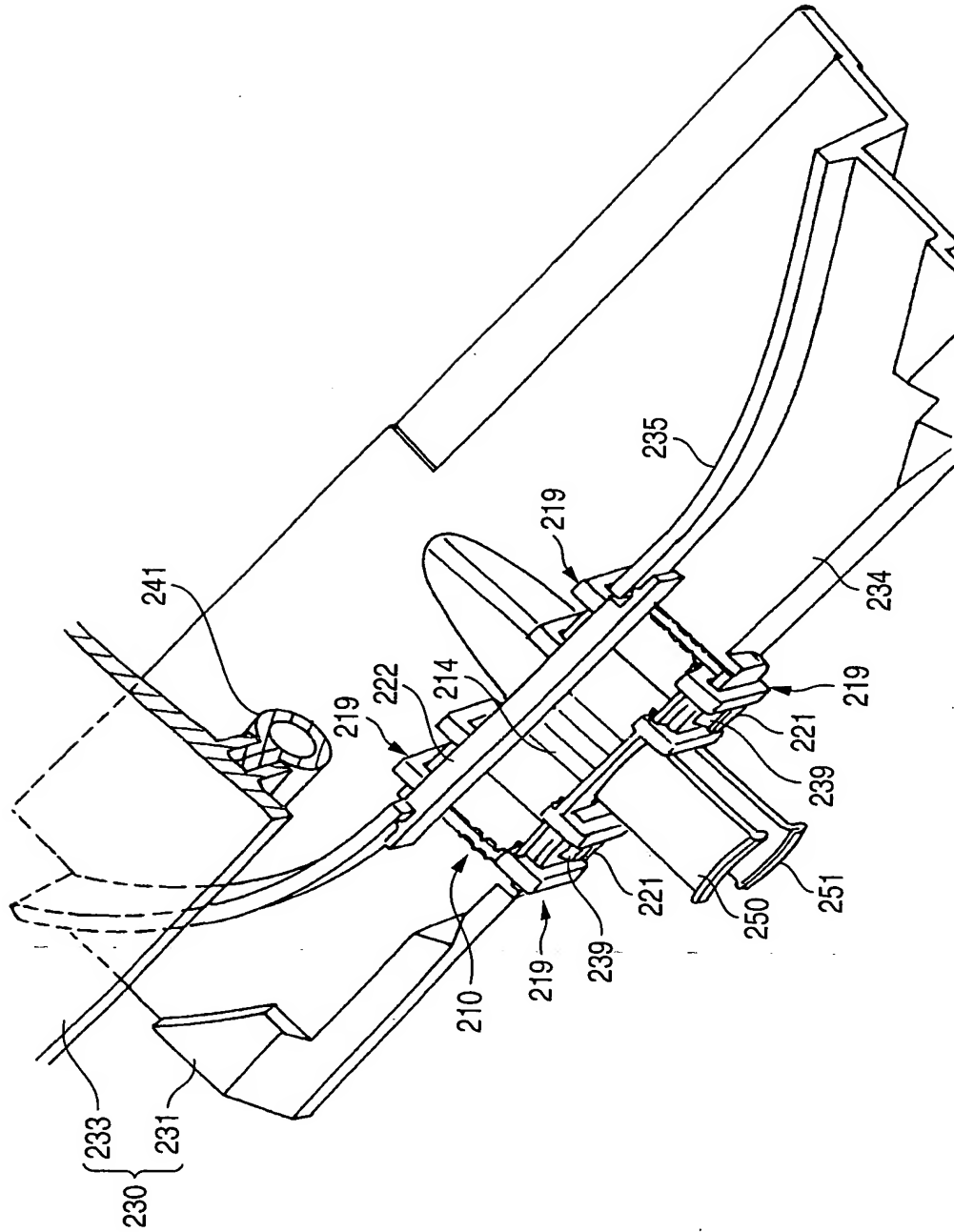






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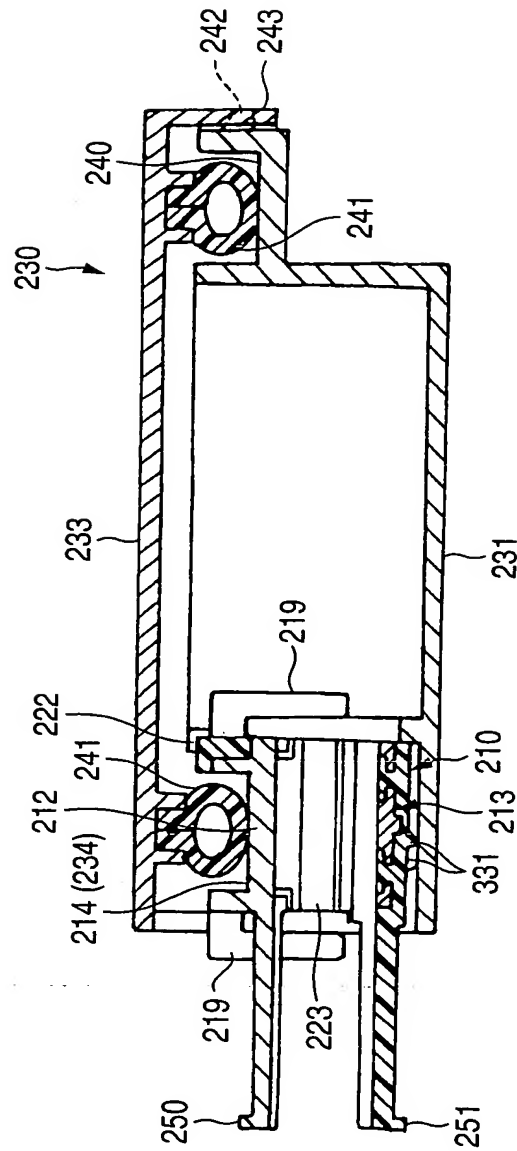
FIG. 20





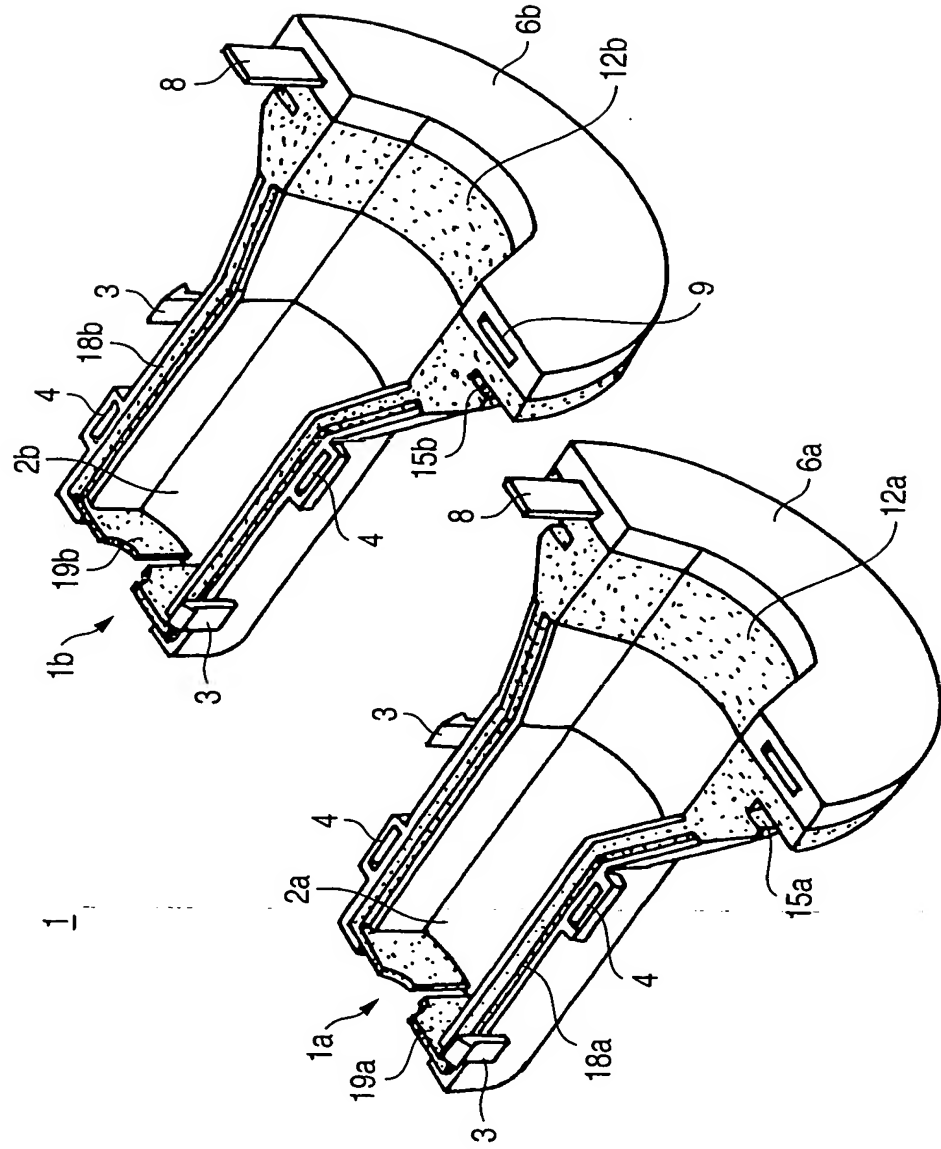
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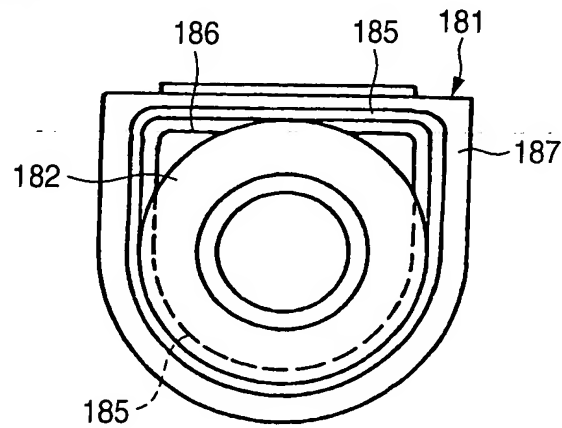
FIG. 21



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FIG. 22





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FIG. 24A

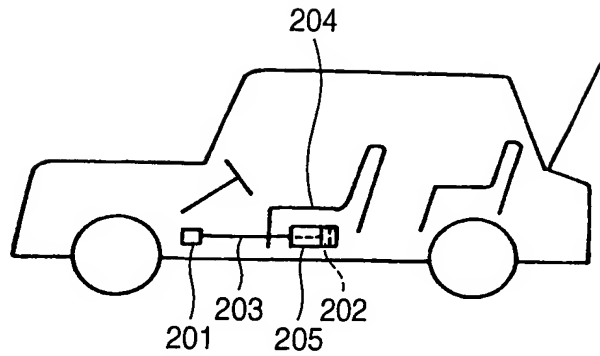
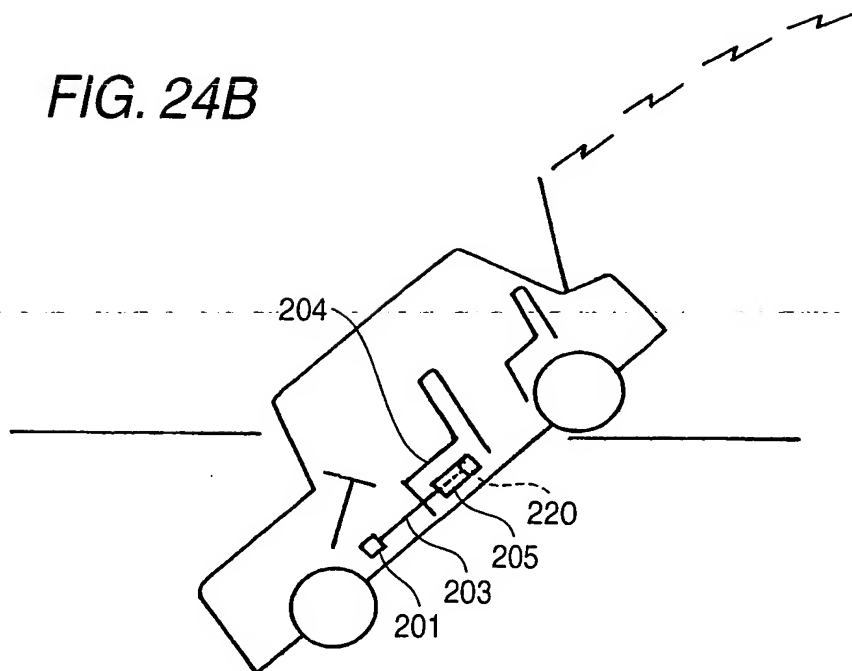


FIG. 24B



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FIG. 25

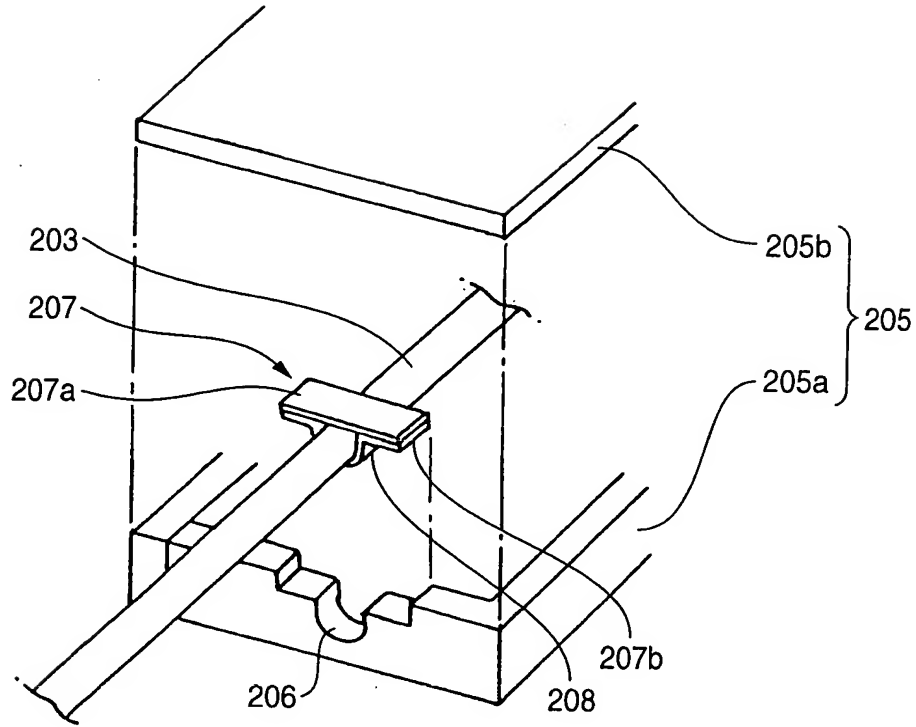


FIG. 26

